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STEPHEN B. ACKERMAN
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
NGUYEN, LONG T	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/631,841
Filing Date: July 31, 2003
Appellant(s): SHIAH, CHUN

Billy J. Knowles
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 6/23/06 appealing from the Office action mailed on 2/21/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

* U.S. 6,373,328	Rapp	04-2002

* Applicant's Admitted Prior Art, Figure 1.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

Response to Amendment

1. The amendment filed 11/28/05 is still objected to under 35 U.S.C. 132 because it still introduces new matter into the original disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the recitations regarding the capacitance values of CHC and Cp such that the coupling ratio of CHC/(Cp + CHC) ≈ 1 recited from line 3 of paragraph [0018] to line 1 of paragraph [0019] recited in the specification filed on 1/14/05 and in claims 10, 21, 31 and 41 (amendment filed on 1/14/05, previously state in the final office action 4/6/05); the limitation regarding the ratio of the large capacitor and the parasitic capacitor approaching unity value recited in independent claims 1, 12, 23 and 33 (amendment filed 1/14/05, previously state in the final office action 4/6/05); and "the capacitance value of the large capacitor is chosen to be very large with respect to a capacitance value of said parasitic capacitor" as recited in claims 11, 22, 32 and 42 (amendment filed on 6/29/05) .

Applicant is required to cancel the new matter in the reply to this Office Action.

Specification

2. The substitute specification filed on 1/14/05 has not been entered because it contains new matter as discussed above.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, at the time the application was filed on 7/31/03, the originally disclosure (filed 7/31/03) does not support the limitation "a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point" as recited in independent claims 1, 12, 23 and 33 (amendment filed on 1/14/05, previously state in the final office action 4/6/05). Furthermore, the original disclosure does not support the limitation regarding the capacitance values of CHC and Cp such that the coupling ratio of CHC/(Cp + CHC) $\approx$ 1 as recited in claim 10, 21, 31 and 41 (amendment filed on 1/14/05, previously state in the final office action 4/6/05), and "the capacitance value of the large capacitor is chosen to be very large with respect to a capacitance value of said parasitic capacitor" as recited in claims 11, 22, 32 and 42 (amendment filed on 6/29/05).

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation "a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value" on lines 5-8 is misdescriptive since it is inconsistent with what is disclosed. Note that, in the amendment filed 1/14/05, lines 3-12 of paragraph [0018] of the specification recites that the ratio of CHC/(Cp + CHC) $\approx$ 1, so the coupling ratio of a capacitance value of the large capacitor (CHC) and a capacitance value of a parasitic capacitor (Cp) approaching a unity value recited on lines 5-8 of claim 1 is misdescriptive. Note that the recitation "a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor" means CHC/Cp (i.e., not CHC/(Cp + CHC)). Clarification and/or appropriate correction is required. Note that the similar problem also exists in independent claims 12, 23, and 33.

Claims 2-11, 13-21 and 34-42 are indefinite because they include the indefiniteness of claims 1, 12, 23 and 33, respectively.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA, Figure 1) in view of Rapp (USP 6,373,328).

Note that Figure 1 of the AAPA discloses an input buffer receiver, which includes: a buffer input portion (100) comprising a bias node (b1) for providing a bias voltage (Vb1), a parasitic capacitor (Cp) connected between the bias node and a ground reference, a first transistor (NMOS N1), a second transistor (PMOS P1), a third transistor (PMOS P2), a fourth transistor (NMOS N2), and a lower supply voltage (Vss); and a buffer output portion (200) in communication with the buffer input portion for producing an output signal (Signal_Out). Figure 1 of the AAPA does not disclose that the input buffer portion (100) including a large capacitor connected between the bias node (b1) and the lower power supply (Vss). However, the Rapp reference discloses in Figure 5 an input buffer portion (76) comprising a large capacitor (90) connecting between a bias node (node connecting gates of transistors 86 and 88 together) and a lower power supply voltage (the source of the transistors 92 and 94) for stabilizing the voltage at the bias node (i.e., the voltage at the gates of transistors 86 and 88 is stabled), see lines 40-42 of Col. 9 of Rapp. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the AAPA by providing a large capacitor connected between the bias node (b1) and the lower supply voltage (Vss which is also connected to the sources of transistors N1 and N2) for the purpose of holding the voltage at the bias node to be stabled (i.e., preventing voltage at the bias node from variations) so as to improve the performance of the circuitry. Thus, this modification meets all the limitations of claims 1-42 because the structure of the modification as discussed is substantially identical to the structure of the claim invention. Note that it is obvious that when designing a circuit, one skill in

the art would like to design the circuit so that the parasitic capacitance of the circuit is as small as possible to reduce noises and delays of the circuitry, and thus the value of the parasitic capacitance is very small compares with the value of large capacitor, and that the ratio of C_large/(C_large + Cp) ≈ 1 would also be met.

(10) Response to Argument

With respect to objection to the amendment filed on 1/14/05 under 35 U.S.C. 132 because it introduces new matter into the disclosure of the invention, Appellant argues (line 15 of page 12 to line 3 of page 14): the original text describes that "because of its large coupling ratio, CHC essentially charges couples the VB11 gate voltage of the PMOS bias node to the VSS source voltage...", and that the coupling ratio would be defined as CR = $C_{HC}/(C_{HC} + C_P)$, and the larger magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P, the coupling ratio approaches a maximum value of unity (1), therefore a large coupling would clearly by any value that approaches unity (1).

In response, the Examiner agrees that the coupling ratio is easily to be derived as CR = $C_{HC}/(C_{HC} + C_P)$, and it is clear that if the large capacitor C_{HC} is much larger than the parasitic capacitor C_P then the coupling ratio CR will approaches 1. However, the original specification failed to recite that the coupling ratio of CR = $C_{HC}/(C_{HC} + C_P)$ is approximately a unity value (1), and the original specification also failed to recite that the large capacitor C_{HC} is much larger than the parasitic capacitor C_P so that the coupling ratio CR will approaches 1. Note that the original disclosure only disclosure the coupling ratio to be $C_{HC}/(C_{HC} + C_P)$ and that C_{HC} is a large capacitor, but did not specifically disclose that the capacitance values of C_{HC} and C_P

are chosen so that the coupling ratio $C_{HC}/(C_{HC} + C_P) \approx 1$. Thus, the amendment filed on 1/14/05 is objected under 35 U.S.C. 132 because it introduces new matter to the disclosure.

With respect to the new matter and the rejection under 35 U.S.C. 112, 1st paragraph, Appellant argues (line 14 of page 4 to line 22 of page 16): the original text describes that "because of its large coupling ratio, C_{HC} essentially charges couples the VB11 gate voltage of the PMOS bias node to the VSS source voltage...", and that the coupling ratio would be defined as $CR = C_{HC}/(C_{HC} + C_P)$, and the larger magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P, the coupling ratio approaches a maximum value of unity (1), therefore a large coupling would clearly by any value that approaches unity (1)., wherein C_{HC} = capacitance of the large capacitor, and C_P = capacitance of the parasitic capacitor.

In response, the Examiner agrees that agrees that the coupling ratio is easily to be derived as $CR = C_{HC}/(C_{HC} + C_P)$, and it is clear that if the large capacitor C_{HC} is much larger than the parasitic capacitor C_P then the coupling ratio CR will approaches 1. However, the original specification failed to recite that the coupling ratio of $CR = C_{HC}/(C_{HC} + C_P)$ is approximately a unity value (1), and the original specification also failed to recite that the large capacitor C_{HC} is much larger than the parasitic capacitor C_P so that the coupling ratio CR will approaches 1. Note that the original disclosure only disclosure the coupling ratio to be $C_{HC}/(C_{HC} + C_P)$ and that C_{HC} is a large capacitor, but did not specifically disclose that the capacitance values of C_{HC} and C_P are chosen so that the coupling ratio $C_{HC}/(C_{HC} + C_P) \approx 1$. Also note that, the original claim also does not have the position that the coupling ratio $C_{HC}/(C_{HC} + C_P) \approx 1$.

With respect to the rejection under 35 U.S.C. 112, 2nd paragraph, Appellant argues that: in claims 1, 12, 23 and 33, a large capacitor is coupled between the bias node and the lower supply voltage "for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point", and the coupling ratio is $C_{HC}/(C_{HC} + C_P)$, (i.e., the coupling ratio is not C_{HC}/C_P).

In response, the recitation "a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor" means $CR = C_{HC}/C_P$ (i.e., ratio of a capacitance value of the large capacitor C_{HC} and a capacitance value of the parasitic capacitor C_P). The above recitation "a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor" does not means $CR = C_{HC}/(C_P + C_{HC})$ because in order to have a ratio of $C_{HC}/(C_P + C_{HC})$, then it should be recited as "a coupling ratio between a capacitance value of said large capacitor and a sum of a capacitance value of a parasitic capacitor and the capacitance of the large capacitor". Clearly, claims 1, 12, 23 and 33 only recite that a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor approaches unity (i.e., $C_{HC}/C_P \approx 1$) and thus these claims are misdescriptive since the amendment filed on 1/14/05 recites that $C_{HC}/(C_{HC} + C_P) \approx 1$.

With respect to the rejection under 35 U.S.C. 103 (Figure 1 of the Applicant Admitted Prior Art (AAPA) in view of Rapp), Appellant argues (line 10 of page 18 to line 18 of page 19) neither AAPA, nor Rapp, nor AAPA in combination with Rapp includes a large capacitor

between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and ground reference point.

In response, as discussed in the 103 rejection, the combination of AAPA and Rapp discloses a large capacitor (90, Figure 5 of Rapp in the combination/modification discussed in the 103 rejection) coupled between the bias node and the lower supply voltage.

Appellant further argues (line 20-23, page 19) that "the large capacitor in Rapp is connected to the ground reference point and does not charge couple the bias node to the lower supply voltage such that the voltage at the biasing node follows the lower supply voltage".

In response, it is seen in Figure 5 of Rapp that the large capacitor (90) is coupled between the bias node (gates of 86 and 88) and a lower supply voltage of the circuit (Figure 5), so when combine with the circuit in Figure 1 of AAPA then the capacitor 90 in Figure 5 of Rapp will be connected between the bias node (b1, Figure 1 of AAPA) and the lower supply voltage Vss of the input buffer 100 (Figure 1 of AAPA), and thus the capacitor (90 in the combination/modification) will charge couple the biasing node b1 to the lower supply voltage Vss.

Appellant further argues (lines 1-6, page 20) that "the circuit of Rapp provides a comparator circuit that compares the voltage value of a programming voltage supply Vpp at node A of Figure 5 of Rapp agains the voltage value of the power supply voltage Vdd. The capacitor of Rapp helps "to hold the voltage constant at the gate of transistor 86" this does not provide the

coupling of the lower supply voltage to the bias node of this invention". In response to appellant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642.F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Note that, as clearly discussed above, when combine the APPA (Figure 1) with Rapp, then the capacitor (90) of Rapp in the above combination will charge coupling the lower supply voltage Vss to the biasing node b1.

Appellant also argues (lines 7-14, page 20) that there is not sufficient basis for conducting that the combination of the claimed elements would have been obvious to one having skilled in the art. In response, this argument is not persuasive because the 103 rejection is clearly recited: The APPA teaches all the limitations of the input buffer receiver except for a large capacitor connected between the bias node and the lower power supply. The Rapp reference teaches an input buffer portion (76) comprising a large capacitor (90) connecting between a bias node (node connecting gates of transistors 86 and 88 together) and a lower power supply voltage (the source of the transistors 92 and 94) for stabilizing the voltage at the bias node (i.e., the voltage at the gates of transistors 86 and 88 is stabled), see lines 40-42 of Col. 9 of Rapp. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the AAPA by providing a large capacitor connected between the bias node (b1) and the lower supply voltage (Vss which is also connected to the sources of transistors N1 and N2) for the purpose of holding the voltage at the bias node to be stabled (i.e., preventing voltage at the bias node from variations) so as to improve the performance of the circuitry. Thus, the 5 steps to construct the 103 rejection are clearly presented

including the motivation for combination also provided. Thus, applicant argument that "there is not sufficient basis for conducting that the combination of the claimed elements would have been obvious to one having skilled in the art" is not found persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

LONG NGUYEN
PRIMARY EXAMINER

Conferees:

Timothy Callahan, SPE

Darren Schuberg, SPE